Laboratory 1

(Due date: **002**: January 25th, **003**: January 26th)

OBJECTIVES

- ✓ Introduce VHDL Coding for FPGAs: Circuit description and testbench generation.
- ✓ Learn the Xilinx FPGA Design Flow with Vivado HL Webpack: Synthesis, Simulation, and Bitstream Generation.
- ✓ Learn how to assign FPGA I/O pins and download the bitstream onto the Nexys™-4 DDR Artix-7 FPGA Board.

VHDL CODING

- ✓ Refer to the Tutorial: VHDL for FPGAs for a list of examples.

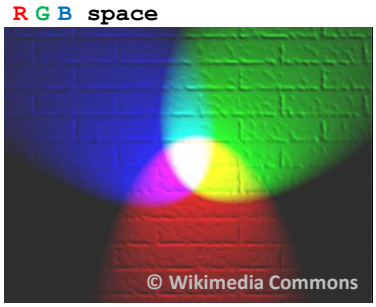
NEXYS™-4 DDR ARTIX-7 FPGA BOARD SETUP

- The Nexys-4 DDR Board can receive power from the Digilent USB-JTAG Port (J6). Connect your Board to a computer via the USB cable. If it does not turn on, connect the power supply of the Board.
- Nexys-4 DDR documentation: Available in class website.

FIRST ACTIVITY (100/100)

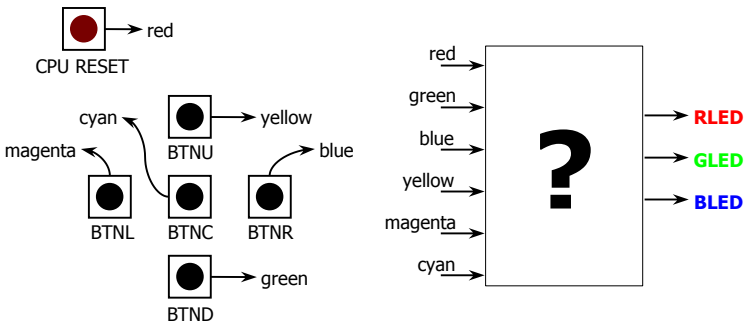
- **RGB LED Control**: A color can be represented by a combination of red (R), green (G), and blue (B) intensities, hence RGB color. An RGB LED includes a red LED, a green LED, and a blue LED, which are controlled independently.

R G B	Color
0 0 0	Black
1 0 0	Red
0 1 0	Green
0 0 1	Blue
1 1 0	Yellow
1 0 1	Magenta
0 1 1	Cyan
1 1 1	White



- In this experiment, we control the maximum intensities of each LED using '1' as the brightest color, and '0' as the darkest color. This produces eight colors.

- Colors are produced via six push-buttons, as shown. Pressing on a button generates a particular color. If no button is pressed, we get Black. If more than one button is pressed, we get White. The circuit '**?**' generates three output signals (RLED, GLED, BLED) based on the six push-buttons.



- **VIVADO DESIGN FLOW FOR FPGAs (follow this order strictly)**:
  - ✓ Create a new Vivado Project. Select the **XC7A100T-1CSG324 Artix-7 FPGA** device.
  - ✓ Write the VHDL code for the circuit '**?**' (use logic gates or *with-select* description). Synthesize your circuit (Run Synthesis).
  - ✓ Write the VHDL testbench to test the circuit: the circuit must generate the eight given colors (via RLED, GLED, BLED).
  - ✓ Perform Functional Simulation (Run Simulation → Run Behavioral Simulation). **Demonstrate this to your TA.**
  - ✓ I/O Assignment: Create the XDC file.
    Nexys-4 DDR Board: Use `BTNU`, `BTNL`, `BTNC`, `BTNR`, `BTND`, `CPU RESET` as inputs, and the red, green, and blue LEDs of the `LD17` component (RGB LED) as outputs. All I/Os are active high, except for `CPU RESET` which is active low.
  - ✓ Implement your design (Run Implementation).
  - ✓ Do Timing Simulation (Run Simulation → Run Post-Implementation Timing Simulation). **Demonstrate this to your TA.**
  - ✓ Generate the bitstream file (Generate Bitstream).
  - ✓ Download the bitstream on the FPGA (Open Hardware Manager) and test. **Demonstrate this to your TA.**

- Submit (as a .zip file) the generated files: VHDL code, VHDL testbench, and XDC file to Moodle (an assignment will be created). DO NOT submit the whole Vivado Project.

TA signature: _____ **Date:** _____

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